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Interfacial Dead-Layer Effects in Hf-Silicate Films with Pt or RuO_2 Gates

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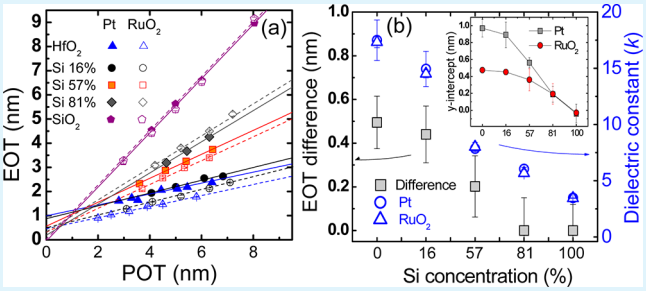
ABSTRACT: The interfacial dead-layer (DL) effects at the interfaces between Hf-silicate films and Pt or RuO_2 gate metals are examined. The Si content in the Hf-silicate film was controlled to vary the dielectric constant (k). The DL effect was strongly dependent on the k value of the Hf-silicate layer, and was suppressed when the Si content was increased to ~80% ($k \approx 6$). This Si content also coincides with the Fermi level pinning-free composition. Therefore, the optimum high-k gate dielectric structure could be a higher-k layer HfO_2 capped with a lower-k layer ($k \approx 6$) with minimum thickness (~1 nm) for the best dielectric performance.



KEYWORDS: *interfacial dead-layer, Hf-silicate, dielectric constant, Pt and RuO_2 gate*

INTRODUCTION

High-k gate dielectrics combined metal gates with an appropriately controlled effective work function (EWF) are now the industry standard for high-performance complementary metal insulator semiconductor field effect transistors (CMISFETs).[1] The thickness of the high-k HfO_2-based dielectric layers has been decreased to ~2 nm, which is assisted by the scavenge effect of active metal gates over the interfacial low-k layer thickness. This has allowed for aggressive scaling of the equivalent oxide thickness (EOT) to <1 nm.[2,3] The authors also reported the scavenge effect of TiN gate electrode over the HfO_2-based gate dielectric stack, which could be further enhanced by adopting La-containing TiN gate.[2] The thinning of the high-k layers eliminates many problems related to defects embedded in the layers, because the total amount of defects decreases with the thinner high-k film thickness for a given density of defects in bulk of the high-k film. Furthermore, the high-k/metal gate will be the gate stack structure for future FinFETs, which underscores their importance. However, the dead-layer (DL) effect, which is associated with the hindrance of ionic polarization near the interface with the metal gate, fundamentally limits the ultimate scaling of EOT into the deep sub1 nm EOT range. It was recently reported that the use of RuO_2 as the gate metal suppressed the DL effect and provided a p-type MISFET with an appropriate EWF.[4]

Other than considerations for the practical aspects of the DL effect for applications, the origin of the effect is not yet clearly understood, and there are certain discrepancies between the theoretical understanding based on ab initio calculations[5] and many experimental results including the authors' own work[4] and model work adopting the epitaxial Pt and $SrRuO_3$ metals on $SrTiO_3$ dielectrics.[6] Detailed discussions on this aspect of DL-related issues are given elsewhere.[4] Although detailed understanding of these discrepancies is still missing, it is quite clear that the DL effect must disappear as the k-value of dielectrics decreases, because the high ionic (or dipolar) polarization of high-k dielectrics compared with the more covalent SiO_2 is basically due to the mutual interaction between the highly polarizable ions.[5,7] The ionic bonding nature of high-k dielectrics induces several problems, such as long-range phonon scattering of carriers in the channel, and Fermi-level pinning at the high-k/metal interface, which is detrimental to the CMISFET operation. Therefore, it is important to understand how low the k-value must be to suppress the DL effect in an MIS structure with high-k dielectrics, and how the gate stack structure can be optimized to alleviate the detrimental effects.

In this work, MIS capacitors were fabricated with Hf-silicate films with varying dielectric constants from 17 (HfO_2) to 3.9 (SiO_2), which was accomplished by changing the cycle ratio during the atomic layer deposition (ALD) of HfO_2 and SiO_2 layers. Either Pt, which induces a severe DL effect, or RuO_2, which has a much milder DL effect, is adopted as the gate metal. The k-value and DL effect were examined using the plot of EOT vs the physical oxide thickness (POT) for a given type of Hf-silicate. EWFs of the two metals were extracted from the plot of the flat band voltage (V_{fb}) as a function of the capacitance equivalent thickness (CET) for each Hf-silicate film with Pt or RuO_2 gates, as a way to measure the Fermi-level pinning and surface trapping.

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EXPERIMENTAL SECTION

Hf-silicate films were deposited on HF-cleaned p-type Si (100) substrates by ALD at a wafer temperature of 270 °C, using tetrakis[ethylmethylamino]hafnium ($Hf[N(CH_3)(C_2H_5)]_4$) and tris-(dimethylamino)silane ($SiH[N(CH_3)_2]_3$) as precursors and ozone gas (concentration of 170 g^{-3}) as the oxygen source. The Si/(Hf+Si) concentration in the Hf-silicate film was controlled from 16 to 81%. ALD HfO_2 and thermally oxidized SiO_2 films were also prepared as references to compare their properties with those of Hf-silicate films. Details about the ALD process can be found elsewhere.[8] The film thickness varied from ~2 to ~8 nm, which was measured by spectroscopic ellipsometry (J. A. Woollam, ESM-300). The 80-nm-thick Pt or 30-nm-thick RuO_2 metal gates were sputter-deposited on the various Hf-silicate films using a metal shadow mask (300 μm hole diameter). Fifty-nanometer-thick Pt was additionally deposited on the RuO_2 gate to improve the contact during probing using a W-tip. To minimize the damage to the dielectric films, the DC power applied to the Pt target (3 in. diameter) was gradually increased from 12 W for 300 s to 15 W for 600 s, 20 W for 600 s, and finally to 100 W for 200 s under an Ar pressure of 1.6×10^{-2} Torr. RuO_2 was deposited under fixed conditions with an RF power of 60 W for 400 s with mixed sputtering gas of Ar (30 sccm) and O_2 (3.5 sccm) at a pressure of 1.5×10^{-2} Torr, where sccm is standard cubic centimeters per minute. These conditions are the optimized conditions for the deposition of RuO_2 on HfO_2.[9] All MIS capacitors were then subjected to forming gas (5% H_2/95% N_2) annealing at 400 °C for 30 min. The atomic concentrations and depth profiles of the films were analyzed by Auger electron spectroscopy (AES, Perkin-Elmer 660). Capacitance–voltage (C–V) characteristics were examined using an HP 4194A at 500 kHz. The measured C–V curves were simulated using Hauser's CVC program to obtain the V_{fb} and EOT values.[10] The gate leakage current density (J_g) was measured using an HP 4145B semiconductor parameter analyzer under gate injection conditions.

RESULTS AND DISCUSSION

Figures 11a and b show the AES depth profiles of Hf-silicate films with Si contents (= Si/[Si+Hf]) of 16 and 56%,

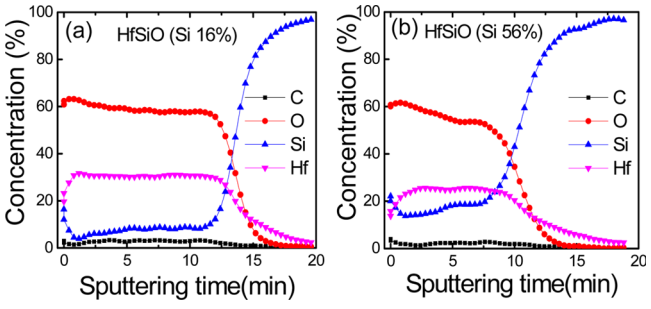

Figure 1. AES depth profiles of as-deposited Hf-silicate films with Si contents (= Si/[Si+Hf]) of (a) 16 and (b) 56%, respectively.

respectively, which indicate that the chemical compositions are relatively uniform along the film thickness direction. Two to three percent carbon residue content is commonly observed. Figure 2a shows the variations in the resistivity and deposition rate of Pt and RuO_2 metals as a function of DC/RF sputtering power. The resistivities of Pt and RuO_2 films adopted in this work are 25 and 35 ohm cm, respectively, and the deposition rate increases linearly with the DC/RF power. Figure 2b shows that Pt metal has a highly ⟨111⟩-preferred growth direction along the direction normal to the film surface (upper panel), whereas RuO_2 has relatively random growth directions (lower panel). The details for RuO_2 growth can be found elsewhere.[9]

Figure 3a shows the variations in EOT as a function of POT for the Hf-silicate films with different Si concentrations for the

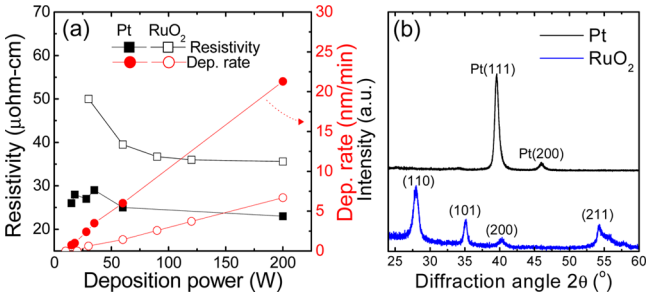

Figure 2. (a) Variations in the resistivity and deposition rate of Pt and RuO_2 metals as a function of sputtering power and (b) XRD spectra of as-deposited Pt and RuO_2 films.

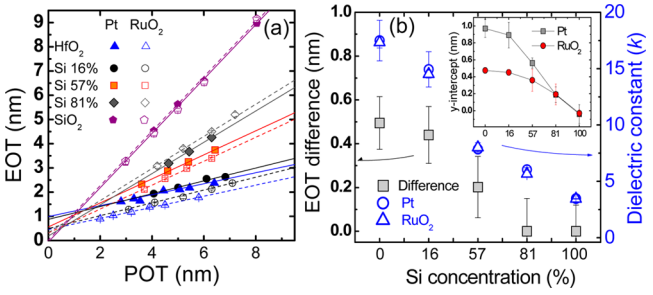

Figure 3. (a) Variation in equivalent oxide thickness (EOT) as a function of physical oxide thickness (POT) for the Hf-silicate films with various Si concentrations in MIS (Pt and RuO_2/Hf-silicate/Si) including HfO_2 and SiO_2 and (b) summary chart from the slopes (k value) and y-axis intercepts (DL effect) of the best-linear fitted graphs (in panel a).

Pt and RuO_2 gates. The slopes and y-axis intercepts of the best linear-fit graphs, which represent the k value and DL effect, respectively, are summarized in Figure 3b. In Figure 3a, the quantum confinement effect of the majority carriers (holes) in the Si substrate, which actually corresponds to the DL effect of the Si-substrate, was already considered during the CVC simulation, so that the y-axis intercept could be 0 if there is no DL effect at the dielectric/metal interface. Several notable findings could be obtained from Figure 3. First, the k-value extracted from the slope of the linear fits of the EOT-POT data follows very well the general trends of highest k at the HfO_2 (~17) and lowest k at the SiO_2 (~4), with intermediate values for the Hf-silicates. More notable is that the k value of a certain Hf-silicate film with a given Si concentration is independent of the types of gate metal used, suggesting that the metal gates have hardly any influence on the bulk property of the dielectrics. Third, the EOT of Hf-silicate films is generally lower with the RuO_2 gate compared with the Pt gate, and the difference diminishes as the Si concentration increases, which is summarized in the left-hand vertical axis of Figure 3b. This is mainly due to the generally higher y-axis intercept values of Pt gated samples when the Si concentration is low, which is summarized in the inset of Figure 3b. This suggests that the DL effect at the interface with Pt is aggravated compared with the RuO_2 gate for the higher Hf concentration. The generally smaller DL effect from the RuO_2 gate compared with the Pt gate is in accordance with many other works.[4,6,11] However, it must be noted that this is not the case when the dielectric film becomes richer in Si concentration. In this case, the critical Si concentration was ~80% (k value ~6). The RuO_2 gate still has the DL effect at the Si concentration of 81%, at which the Pt

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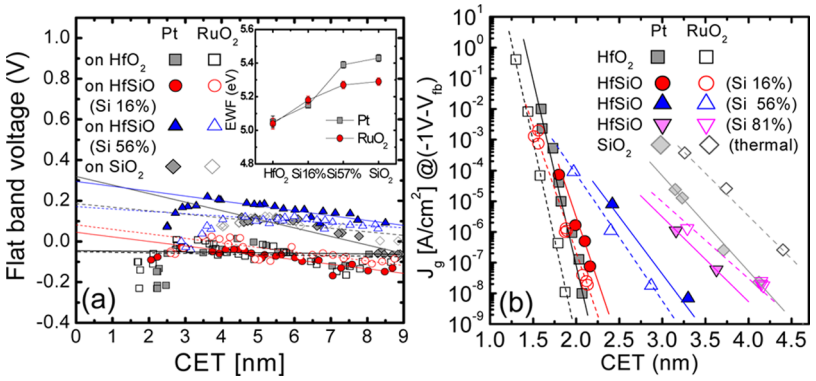

Figure 4. (a) Variation in V_{fb} as a function of CET for the various Hf-silicate films having Pt or RuO_2 electrodes and (inset) the EWF values extracted from the *y*-axis intercepts of V_{fb}-CET graph and (b) the J_g vs CET graph of the various dielectrics with Pt and RuO_2 electrodes.

gate has the same degree of DL effect. The DL effects for both electrodes almost completely disappear only at the SiO_2.

DL effect must be lower for Pt electrode compared with the RuO_2 electrode on highly polarizable dielectrics,[4] such as HfO_2, based on theoretical considerations,[5,12] which is in a stark contrast to the experimental results (Figure 3). This suggests that there is some unidentified process that influences the DL effect at the interface with metals during the gate fabrication process. This unidentified process may have something to do with the surface damaging effect and related defect generation, which becomes more serious for the more ionically bonded surface of HfO_2 than the more covalently bonded surface of SiO_2. The surface damage effect may induce a very thin chemically modified layer with a lower *k* value. The more dominant damaging effect by Pt deposition on the ionically bonded surface compared with the covalently bonded surface can be supported by the data shown in Figure 4.

Figure 4a shows the variations in V_{fb} as a function of CET for the various Hf-silicate films with Pt or RuO_2 gates. For these measurements, a terraced SiO_2 wafer was prepared by wet etching technique,[9] and ~2 nm-thick Hf-silicate films with different Si concentrations were deposited. When the V_{fb} values in the CET range of $\gtrsim$3 nm are best-linearly fitted, the *y*-axis intercept gives information on the EWF of Pt and RuO_2 gates for different Hf-silicates. The extracted EWF data are summarized in the inset of Figure 4a. It is notable that the Pt and RuO_2 gates have an almost identical EWF when the dielectric was HfO_2 and Hf-silicate with a Si concentration of 16%. This is perhaps due to the Fermi level pinning effect by the produced surface states on the more ionically bonded surfaces. In contrast, when the Si concentration was > ~57%, Pt and RuO_2 show EWF values of 5.4 and 5.3 eV, respectively, suggesting an almost complete lack of pinning effect. This contrasts to the classical theory on the surface Tamm states by Mead[13] and Kurtin,[14] which states that the more ionically bonding dielectric surface must show more pinning-free behavior compared with more covalently bonded dielectric surfaces. However, this classic theory is based on the understanding that the surface states on the ionic-bonding materials are concentrated near the band edges, whereas those on the covalently bonded materials mostly reside near the center of the band gap. In this experiment, the chemically inert nature of Pt and RuO_2 metals and strong covalent Si−O bonds results in a negligible density of trap (or defect) states near the interface, so the pinning effect is minimized. In contrast, the Hf−O bonding on the Hf-richer dielectric surfaces are vulnerable to trap generation, perhaps due to oxygen vacancy generation, which induces deep trap states,[15] making the Fermi level of the gate metals pin to the trap locations in the band gap. This is in a good agreement with the observation of the higher DL effect for the samples richer in Hf in Figure 3.

Figure 4b shows the J_g vs CET performance of the various dielectrics with Pt and RuO_2 gates. For this experiment, the samples of Figure 3a were used, and J_g was collected at V_{fb} − 1 V with the metal gate being negatively biased (accumulation condition). The J_g level for the high CET region ($\gtrsim$3 nm), which corresponds to the high Si concentration ($\gtrsim$60%), is generally higher for the RuO_2 gate compared with the Pt gate. This can be understood from the higher EWF of Pt compared with RuO_2 on these dielectrics, which results in a higher Schottky barrier height at the metal/dielectric interface. However, as the CET decreases, or the Hf concentration increases, the EWF of the two metals converges to the same level (~5.0 eV for HfO_2), so the Schottky barrier height must be identical. Then, there must be no gain for J_g, whereas only CET degradation is expected from the Pt-gated samples, which is indeed the case, as shown in Figure 4 (b).

CONCLUSION

In conclusion, the influence of dielectric the dead-layer at the metal/high-*k* gate dielectric interface was examined using Hf-silicates with Pt or RuO_2 as the gate metal. In accordance with previous experimental results, but in contrast to previous theoretical results, Pt has a more significant DL effect compared with RuO_2 when the Si concentration is low (<~80%). The Hf-silicate film with a *k* value as low as ~6 (Si concentration ~81%) still showed the DL effect, although it was much weaker than that for HfO_2, but the difference between the DL effects from Pt and RuO_2 electrodes disappears at this composition. SiO_2 shows negligible DL effect for both electrodes. Considering the variation in the EWF of Pt and RuO_2 on different Hf-silicates, and the accompanying Fermi level pinning effect, the degraded DL effect of the Pt gate compared with the RuO_2 might originate from the chemical modification and defect generation on the surface of ionic-bonded HfO_2. Therefore, a gate stack structure with a higher-*k* HfO_2 layer at the bottom portion capped with a Hf-silicate with a lower *k*-value of ~5−6 (thickness <1 nm) might be optimal for avoiding the surface damage effect during gate formation. Carefully controlled interfacial layer between the higher-*k* layer and Si substrate could be adopted to further improve the higher-*k* layer quality.[16]

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Notes

The authors declare no competing financial interest.

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REFERENCES

(1) Robertson, J. *Rep. Prog. Phys.* **2006**, *69*, 327−396.
(2) Kim, H. K.; Lee, S. Y.; Yu, I.-H.; Park, T. J.; Choi, R.; Hwang, C. S. *IEEE Electron Device Lett.* **2012**, *33*, 955−957.
(3) Choi, C.; Lee, J. C. *J. Appl. Phys.* **2010**, *108*, 064107.
(4) Kim, H. K.; Yu, I.-H.; Lee, J. H.; Park, T. J.; Hwang, C. S. *Appl. Phys. Lett.* **2012**, *101*, 172910.
(5) Stengel, M.; Spaldin, N. *Nature* **2006**, *443*, 679−682.
(6) Boesch, D. S.; Son, J.; LeBeau, J. M.; Cagnon, J.; Stemmer, S. *Appl. Phys. Exp.* **2008**, *1*, 091602.
(7) Black, C. T.; Welser, J. J. *IEEE Trans. Electron Devices* **1999**, *46*, 776−780.
(8) Kim, H. K.; Jung, H.-S.; Jang, J. H.; Park, J.; Park, T. J.; Lee, S.-H.; Hwang, C. S. *J. Appl. Phys.* **2011**, *110*, 114107.
(9) Kim, H. K.; Yu, I.-H.; Lee, J. H.; Park, T. J.; Hwang, C. S. *ACS Appl. Mater. Interfaces* **2013**, *5*, 1327−1332.
(10) Hauser, J. R.; Ahmed, K. *AIP Conf. Proc* **1998**, *449*, 235−239.
(11) Hwang, C. S. *J. Appl. Phys.* **2002**, *92*, 432−437.
(12) Lee, B.; Lee, C.-K.; Han, S.; Lee, J.; Hwang, C. S. *J. Appl. Phys.* **2008**, *103*, 024106.
(13) Mead, C. A. *Solid-State Electron.* **1966**, *9*, 1023.
(14) Kurtin, S.; Mead, C. A. *J. Phy. Chem. Solids* **1968**, *29*, 1865.
(15) Cho, E.; Lee, B.; Lee, C.-K.; Han, S.; Jeon, S. H.; Park, B. H.; Kim, Y.-S. *Appl. Phys. Lett.* **2008**, *92*, 233118.
(16) Li, S.; Han, L.; Chen, Z. *J. Elctrochem. Soc.* **2010**, *157*, 221.